

Firmware Updates

For more information, contact our team on - technical.support@sonifex.co.uk

RB-VHDMA8, RB-VHEMA8, RB-VHCMA4 & RB-VHCMD16		
Versions for units running V0.X.X		
Firmware Versions		
Version	Changes	Description
V0.4.0 / FPGA V0.3.0	Updated	Drivers updated to latest versions
V0.4.0 / FPGA V0.3.0	Added	Front panel lock persistence option
V0.4.0 / FPGA V0.3.0	Added	Front panel lock settable via front panel (hold bank, group, status buttons for 5 seconds)
V0.4.0 / FPGA V0.3.0	Updated	Soft core components updated to latest versions
V0.3.6	Fixed	Fatal error when updating units due to incorrect memory mapping
V0.3.6	Fixed	Issue with initialising AIM-AD daughter boards
V0.3.5	Changed	Reduced default front panel LED brightness slightly
V0.3.5	Added	Front panel brightness control via remote control
V0.3.5	Fixed	Audio freeze when SRC disabled and input loses lock
V0.3.4 / FPGA V0.2.9	Added	New driver for AIM-DD card with selectable termination
V0.3.4 / FPGA V0.2.9	Fixed	De-embed routing error
V0.2.7 (FPGA)	Fixed	Audio routing error introduced in V0.2.6
V0.3.1 / FPGA V0.2.6	Changed	Default IP reverted to 192.168.0.100 and gateway to 192.168.0.1
V0.3.1 / FPGA V0.2.6	Fixed	HD Luma/Chroma streams misalignment during locking
V0.2.4/5 (FPGA)	Internal	Internal versions, not released
V0.3.0 / FPGA V0.2.3	Added	Multiple TCP/IP connections supported
V0.3.0 / FPGA V0.2.3	Added	RWC command for write permission
V0.3.0 / FPGA V0.2.3	Added	WAL command to change login details
V0.3.0 / FPGA V0.2.3	Added	GAC command to retrieve admin connections
V0.3.0 / FPGA V0.2.3	Updated	TCP/IP stack updated
V0.3.0 / FPGA V0.2.3	Improved	Message handling for UART, TCP, UDP
V0.3.0 / FPGA V0.2.3	Changed	Default IP changed to 192.168.1.2 and gateway to 192.168.1.1
V0.3.0 / FPGA V0.2.3	Changed	CLR command resets login details
V0.3.0 / FPGA V0.2.3	Changed	Bank channel button hold disabled in bank mode
V0.3.0 / FPGA V0.2.3	Improved	FPGA/firmware update process
V0.3.0 / FPGA V0.2.3	Changed	Channel status handling optimized (round robin updates)
V0.3.0 / FPGA V0.2.3	Other	Minor improvements
V0.3.0 / FPGA V0.2.3	Fixed	Channel status for channels 2 and 4 de-embedded correctly
V0.2.1 / FPGA V0.2.2	Fixed	Corrected clock phase info for HD audio packets
V0.2.1 / FPGA V0.2.1	Fixed	Corrected parity bit in SD audio packets
V0.2.1 / FPGA V0.2.0	Updated	Rebuild for new CPU soft core with updated drivers
V0.2.1 / FPGA V0.2.0	Improved	SDI locking improved
V0.2.1 / FPGA V0.2.0	Fixed	SCId memory leak
V0.2.1 / FPGA V0.2.0	Other	Minor fixes and changes
V0.2.1 / FPGA V0.2.0	Fixed	Corrected data block numbering in audio packets
V0.2.1 / FPGA V0.2.0	Added	New CPU soft core version
V0.2.1 / FPGA V0.2.0	Improved	SDI locking improved
V0.1.8 / FPGA V0.1.1	Release	Initial release

SONIFEX

Audio Solutions for AV
& Broadcast Media